What is claimed is:

1. A tunneling leakage current compensation circuit, comprising:

a current mirror coupled to a tunneling leakage monitor, said tunneling leakage monitor including a tunneling leakage monitoring device, said current mirror adapted to force a tunneling leakage current of said tunneling leakage device to a predetermined current value; and

a voltage buffer coupled to said leakage monitor, said voltage buffer adapted to generate an output voltage based on a voltage level developed across said leakage monitoring device when said tunneling leakage current is at said predetermined current value.

2. The circuit of claim 1, wherein said current mirror includes an adjustable current source and means to adjust a current generated by said current source.

3. The circuit of claim 2, wherein said current source is a band gap current source.

4. The circuit of claim 2, wherein said means to adjust a current generated by said current source is a digital to analog converter.

5. The method of claim 4, further including a fuse array, said fuse array adapted to apply input signals to inputs of said digital to analog converter based on a state of fuses in said fuse array or a field programmable gate array, said field programmable gate array adapted to apply input signals to inputs of said digital to analog converter based on a programming of said field programmable gate array.

6. The circuit of claim 1, further including a voltage regulator coupled to said voltage buffer, said voltage regulator adapted to supply a fixed voltage to a power distribution network of an integrated circuit chip based on said output voltage of said voltage buffer.

7. The circuit of claim 1, wherein said leakage monitor device is a gate capacitor.

8. A method of compensating for tunneling current leakage in an integrated circuit chip, the method comprising:

forcing a current of known value through a tunneling current leakage monitor device to provide a voltage signal; and

regulating an on-chip power supply of said integrated circuit chip based on said voltage signal.

9. The method of claim 8, wherein said tunneling current leakage monitor device is a gate capacitor.

10. The method of claim 8, further including programming fuses or a field programmable gate array in order to set said value of said known current.

11. The method of claim 8, further including performing a burn-in test of said integrated circuit chip while forcing said current of known value through a tunneling current leakage monitor device.

12. The method of claim 8, wherein said current of known value is selected to be about equal to the tunneling leakage current of a worst-case process integrated circuit chip.

13. The method of claim 8, further including lowering a voltage level of said on-chip power supply for a best-case process integrated circuit chip from a nominal value for a nominal-case process integrated circuit chip and raising said voltage level of said on-chip power supply for a worst-case process integrated circuit chip from said nominal value.

14. The method of claim 8, further including:

selecting a first value for said current of known value for burn-in operation of said integrated circuit that is higher than a second value for said current of known value for normal operation of said integrated circuit; and

determining a voltage level of a burn-in power supply based on said first value.

15. A method of compensating for tunneling current leakage in an integrated circuit chip, the method comprising:

providing a current mirror coupled to a tunneling leakage monitor, said tunneling leakage monitor including a tunneling leakage monitoring device, said current mirror for forcing a tunneling leakage current of said tunneling leakage device to a predetermined current value; and

providing a voltage buffer coupled to said leakage monitor, said voltage buffer for generating an output voltage based on a voltage level developed across said leakage monitoring device when said tunneling leakage current is at said predetermined current value.

16. The method of claim 15, wherein said current mirror includes a current source and means for adjusting a current generated by said current source.

17. The method of claim 16, wherein said means for adjusting said current generated by said current source is a digital to analog converter.

18. The method of claim 17, further including providing a fuse array, said fuse array for applying input signals to inputs of said digital to analog converter based on a state of fuses in said fuse array or providing a field programmable gate array, said field programmable gate array for applying input signals to inputs of said digital to analog

converter based on a programming of said field programmable gate array.

19. The method of claim 15, further including providing a voltage regulator coupled to said voltage buffer, said voltage regulator for supplying a fixed voltage to a power distribution network of an integrated circuit chip based on said output voltage of said voltage buffer.

20. The method of claim 15, wherein said tunneling leakage monitoring device is a gate capacitor.